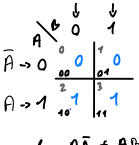
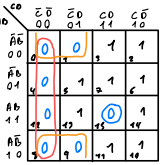
SOP (M) Mar



$f = A\bar{B} + AB$
$= A(\bar{B} + B)$
$= A \cdot 1$
$= A$

POS (M) Min

$Q = \pi(0,1,4,8,9,12,15)$



$\bar{f} = \bar{C}\bar{D} + \bar{A}\bar{C} + ABCD$

$f = \overline{\bar{C}\bar{D} + \bar{A}\bar{C} + ABCD}$

$f = (\overline{\bar{C}\bar{D}})(\overline{\bar{B}\bar{C}})(\overline{ABCD})$

$f = (\bar{\bar{C}} + \bar{\bar{D}})(\bar{\bar{B}} + \bar{\bar{C}})(\bar{A} + \bar{B} + \bar{C} + \bar{D})$

$f = (C+D)(B+C)(\bar{A} + \bar{B} + \bar{C} + \bar{D})$

Boolean Algebra

$x \cdot 0 = 0 \quad x + 0 = x \quad x \cdot x = x \quad x + x = x$

$x \cdot 1 = x \quad x + 1 = 1 \quad x \cdot \bar{x} = 0 \quad x + \bar{x} = 1$

$x \cdot (y+z) = x \cdot y + x \cdot z \leftrightarrow x + y \cdot z = (x+y) \cdot (x+z)$

$x + x \cdot y = x \leftrightarrow x \cdot (x+y) = x$ → Absorption

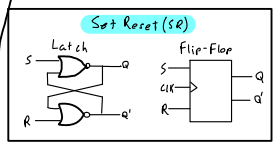
$x \cdot y + x \cdot \bar{y} = x \leftrightarrow (x+y) \cdot (x+\bar{y}) = x$ → Combining

$\overline{x \cdot y} = \bar{x} + \bar{y} \leftrightarrow \overline{x+y} = \bar{x} \cdot \bar{y}$ → Demorgan's Theorem

$x + \bar{x} \cdot y = x + \leftrightarrow x \cdot (\bar{x} + y) = x \cdot y$ → Consensus

Counter Stuff

Set Reset (SR) Latch / Flip-Flop



Un-Signed

0 → 255

$1\,0\,0\,0\,1\,0\,1\,1$ (7 6 5 4 3 2 1 0)

$2^7 + 2^3 + 2^1 + 2^0$

$= 139_{10}$

Signed

-128 → 127

$1\,1\,1\,0\,1\,0\,1\,1$ (7 6 5 4 3 2 1 0)

$= (-2^7) + 2^6 + 2^5 + 2^3 + 2^1 + 2^0$

$= -42_{10}$

$0\,0\,0\,1\,0\,1\,0\,0$ (7 6 5 4 3 2 1 0)

$+ 2^4 + 2^2 = 20_{10}$

1's complement: flip all bits — 0111 ⇒ 1000

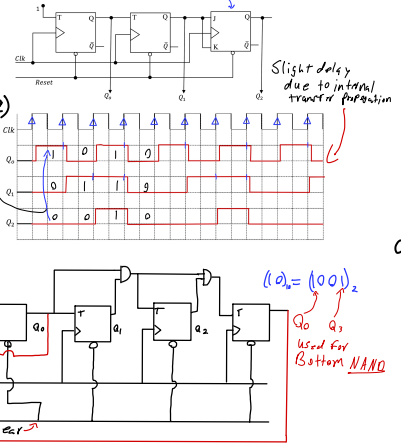
2's complement: flip all bits then add 1 — 0111 ⇒ 1001

SOP = POS

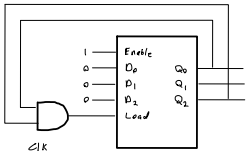
POS: $(\ldots+\ldots)\cdot(\ldots+\ldots)$

SOP: $(\ldots\cdot\ldots)+(\ldots\cdot\ldots)$

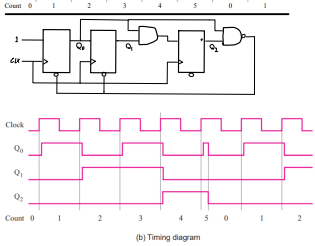
Q1



c)



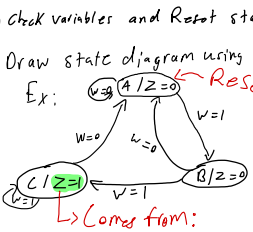
d)



Q2 Steps for VHDL

1. Check variables and Reset state
2. Draw state diagram using ELSEIF

Ex:



3. State table

present $Y_1 Y_0$	Next state W=0 $Y_1 Y_0$	Next state W=1 $Y_1 Y_0$	output [Z]
A 00	A 00	B 01	0
B 01	A 00	C 10	0
C 10	A 00	C 10	1
D 11	/ 0	/ 0 0	0

→ No actual values since No "D" Var in VHDL

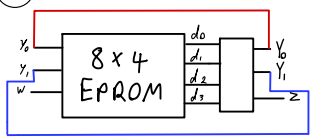
4. EPROM Table

only applied when W=1

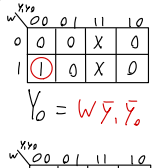
Address W Y_1 Y_0	d_3	d_2 (Z)	d_1 (Y_1)	d_0 (Y_0)
0 0 0	/	0	0	0
0 0 1	/	0	0	0
0 1 0	/	0	0	0
0 1 1	/	X	X	X
1 0 0	/	0	0	1
1 0 1	/	0	1	0
1 1 0	/	1	1	0
1 1 1	/	X	X	X

→ $Z = Y_1 \bar{Y}_0$

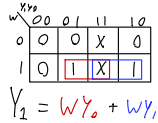
5. → Schematic



6. → K-maps

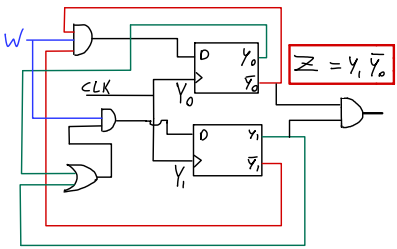


$Y_0 = W\bar{Y}_1\bar{Y}_0$



$Y_1 = WY_0 + WY_1$

7. → D Flip-flops



Q3 FSM

$T_x = Y_x + Y_x$

Input state: Mealy — Present state: Moore

Present $Y_1 Y_0$	W=0 Next $Y_1 Y_0$	W=0 $T_1 T_0$	W=1 Next $Y_1 Y_0$	W=1 $T_1 T_0$	Output Z_1	Z_0
0 0	0 0	0 0	0 1	0 1	0	0
0 1	1 0	1 1	0 1	0 0	0	1
1 0	1 0	0 0	1 1	0 1	1	0
1 1	0 1	1 0	1 1	0 0	0	0

$Z_0 = \bar{Y}_1 Y_0$

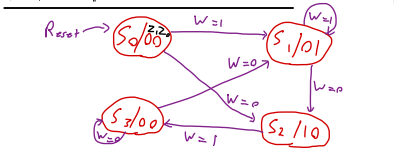
$Z_1 = Y_1 \bar{Y}_0$

Excitation tables

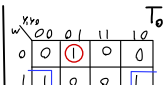
O_n	O_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Truth table

T	Out
0	O_n No change
1	$\bar{O}_n$ Toggle

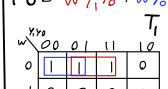


T_0

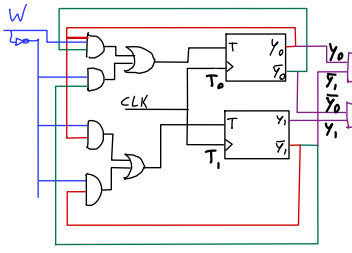


$T_0 = \bar{W}\bar{Y}_1 Y_0 + W\bar{Y}_0$

T_1



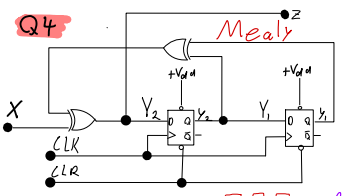
$T_1 = \bar{W}Y_0 + \bar{W}\bar{Y}_1$



Shazzat

Legend

Q4



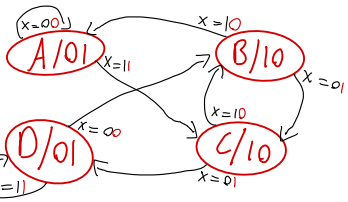
Logic EQ's

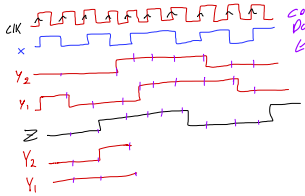
$Y_2 = Y_1 \oplus Y_2 \oplus X$

$Y_1 = Y_2$

$Z = Y_2$

Present $Y_2\ Y_1$	Next $X=0$ $Y_2\ Y_1$	Next $X=1$ $Y_2\ Y_1$	Output Z
A 0 0	A 0 0	C 1 0	0
B 0 1	C 1 0	A 0 0	1
C 1 0	D 1 1	B 0 1	1
D 1 1	B 0 1	D 1 1	0





given

given #'s from Q

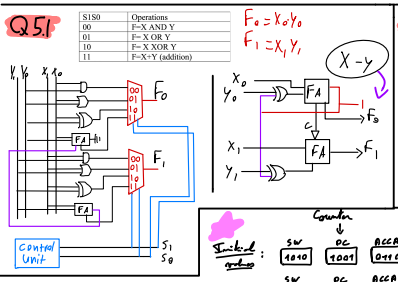
State	B	A	A	C	D	D	D	B	A	A
X	1	0	1	0	1	1	0	1	0	1
Z	0	0	1	1	1	1	0	0	0	1

Q5.1

S1S0	Operations
00	F=X AND Y
01	F= X OR Y
10	F= X XOR Y
11	F=X+Y (addition)

$F_0 = X_0 Y_0$

$F_1 = X_1 Y_1$

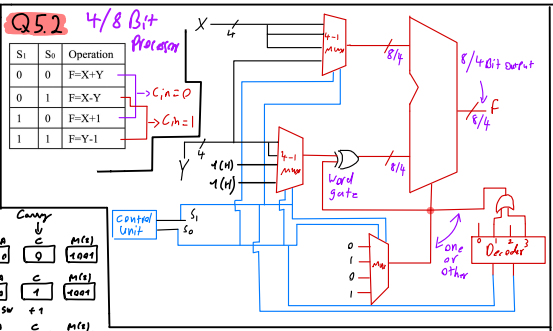


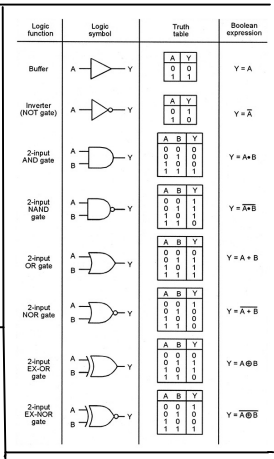
Q5.2 4/8 Bit Processor

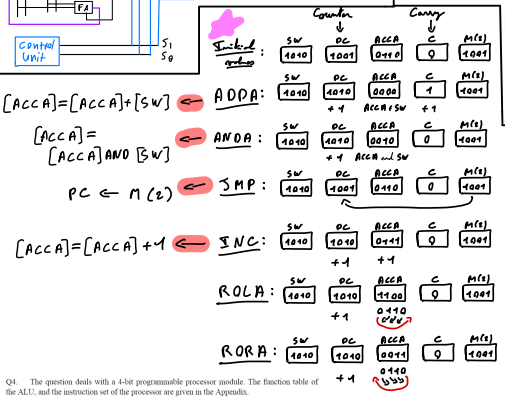
S_1	S_0	Operation
0	0	F=X+Y
0	1	F=X-Y
1	0	F=X+1
1	1	F=Y-1

$\rightarrow C_{in}=0$

$\rightarrow C_{in}=1$







Q1 The question deals with a 4-bit programmable processor module. The function table of the ALU, and the instruction set of the processor are given in the Appendix.

Determine the contents of the Program Counter (PC), Accumulator (ACCA), and the Carry Bit (C) after the execution of each of the following instructions using the given initial values of the Input Switches (Sw), Carry Bit (C), Program Counter (PC), Accumulator (ACCA) and content of the Memory Location 2 (M(2)).

Instruction Set

Mnemonics	Description	Opcode
Register Transfer		
LDR1	Load R1 from input; R1=INPUT	0
LDRC	Load RC from input; RC= INPUT	1
Arithmetic Operations:		
ADDA	Add R1 to Acc; Acc= Acc + R1	2
SUBA	Sub R1 from Acc; Acc= ACC-R1	3
INCA	Increment Acc; Acc=Acc + 1	4
DECA	Dec Acc; Acc= Acc -1	5
DEC-RC	Dec RC; RC= RC-1	6
Logic Operations		
ANDA	And Acc with R1; Acc=Acc&R1	7
ORA	Or Acc with R1; Acc = Acc | R1	8
XORA	XOR Acc with R1; Acc =Acc XOR R1	9
NAND	Invert Acc; Acc = Acc NAND R1	A
SLA	Shift Left Acc; Acc=Acc*2	B
SRA	Shift Right Acc; Acc = Acc/2	C
Control flow		
BNEQZ	branch to start if RC !=0; goto state	D

Q5. Write a program to perform X1+Y1 and set the MSB and LSB to 1.

10101

MSB LSB

```
LDR1   0
ANDA   R1
LDR1   X1
ADDA   R1
LDR1   Y1
```

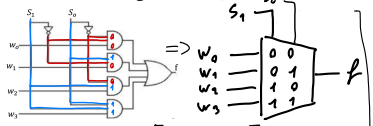
ADDA R1 X1+Y1 (One or the other)

SUBA R1 X1-Y1

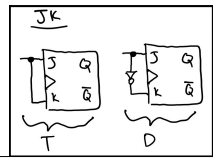
LDR1 81H

ORA R1 (For 8 bit only!)

Multiplexer (MUX)

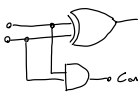


$f = W_0 \overline{S_1}\,\overline{S_0} + W_1 \overline{S_1} S_0 + W_2 S_1 \overline{S_0} + W_3 S_1 S_0$



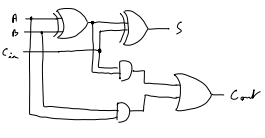
Half Adder:

x	y	Sum	Carry
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

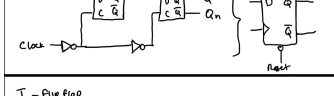


Full Adder:

C_{in}	x_1	x_2	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

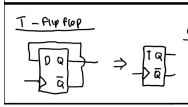


D - Flip flop



$\overline{R}$	CLK	D	Q	$\overline{Q}$	
0	X	X	0	1	Reset
1	0	X	last Q	last $\overline{Q}$	store
1	1	X	last Q	last $\overline{Q}$	
1	↓	0	0	1	update
1	↓	1	1	0	

T - Flip flop



CLK	T	Q	
1	0	No change	Truth Table (T)
↓	1	Toggle	
0	0	No change	
↓	1		

Q_n	Q_{n+1}	T	
0	0	0	Excitation Table (T)
0	1	1	
1	0	1	
1	1	0	